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RESEARCH ARTICLE

Energy-Efficient Aggressive Duty-Cycling of V-Band Power Amplifiers

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ABSTRACT In addition to implementing the core functionality, a design goal for modern circuits is reduced energy consumption. When options for improving active state efficiency are eventually exhausted, the next step is to aggressively minimize the duration a circuit is active to reduce overall energy consumption. Consequently, this article presents a top-down study on efficient duty-cycling of power amplifiers (PAs), spanning system-level considerations down to experimental measurements of a proposed V-band PA. A thorough analysis of the duty-cycling characteristics in a wireless transmitter reveals the significance of fast and efficient switching, particularly if minimal latency is desired and if energy consumption should scale linearly with required data rate. To be able to assess PAs in that regard, the related key characteristics as well as transient RF power measurements are discussed. To enable aggressive duty-cycling at circuit level, the switching process is studied for integrated millimeter-wave (mmWave) class-E PAs. Despite intrinsic switched mode operation at RF, transitions from sleep to active state are not instantaneous, but two phases are revealed: operating point switching (OPS) and large-signal rise in the load network. A kick-starter circuit for speeding up this transition is investigated. To prove these concepts, a two-stage 51 GHz 14 dBm SiGe PA capable of fast and efficient operational state switching is designed and fabricated. Its duty-cycling performance is measured in detail for both single-tone and modulated signals showing turn-on times in the nanosecond range. The results demonstrate highly efficient duty-cycling of data transmission at a cycle duration of just 1 µs for minimum latency. This article aims to allow system and circuit designers to better evaluate requirements for and performance of switchable mmWave PAs in context of duty-cycled communications.

INDEX TERMS BiCMOS integrated circuits, duty-cycling, class-E, mmWave, power amplifiers, transmitter.

I. INTRODUCTION

Battery lifetime of wireless connected devices heavily depends on the energy consumption of their transmitter (TX). To minimize the consumption, the most straightforward approach is to increase the dc-to-RF efficiency η_{active} in active state. However, this is eventually limited by technology and only relevant while the TX is utilized. Any timespan during which it is active despite no data being transmitted results in wasted energy regardless of η_{active}. Hence, when the maximum data rate is not required, the TX is usually duty-cycled at the cost of introducing additional latency. This means only enabling the TX periodically for a short timespan to transmit aggregated data frames. For battery-operated

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wireless sensor nodes with low data rates, this can greatly increase the battery lifetime [1], [2]. But also for high data rate applications, duty-cycling of the TX enables scaling energy consumption with the actually required data rate [3]. This is especially interesting for millimeter-wave (mmWave) communications, where it is possible to achieve compact device dimensions for highly integrated designs [4], [5], [6] well suited for wireless sensor nodes. Here, high data rates are achievable [7], but at the same time, circuits generally have a low efficiency and consequently a high energy consumption. For instance, power amplifiers (PAs) in the V-band (40 GHz to 75 GHz) generally have a peak power-added-efficiency (PAE) below 40 % [8]. The combination of high available data rate that is not always required and high active energy consumption makes duty-cycling very attractive. However, it can lead to very short active timespans if only few bytes are to be transmitted and latency should remain low. The more aggressive the duty-cycling, i.e. the shorter the active timespan, the more important efficient and fast switching behavior becomes.

Additionally, when aggressively duty cycling the TX, a modulation scheme which carries little information in the amplitude is beneficial, because this inflicts less strict requirements on the active state. Ideally, a modulation scheme with low envelope variation after transmit filtering is used. For instance, $\frac{\pi}{4}$-differential quadrature phase-shift keying (DQPSK) as used in Bluetooth enhanced data rate [9] has low envelope variation, which is only present due to root-raised-cosine (RRC) pulse shaping. Even more suitable are for example offset quadrature phase-shift keying (O-QPSK) with half-sine pulse shaping, which is frequently used in wireless sensor networks [10], [11], and gaussian minimum-shift keying (GMSK). Both exhibit a fully constant envelope. Alternatively, on-off keying (OOK) can be attractive due to its simple implementation and energy-efficient demodulation based on envelope detection [5], [6], [12]. But it is highly susceptible to interferers [12] and suffers from local-oscillator feed-through in the output spectrum [13].

Circuitry for duty-cycling has been extensively studied for low-frequency low-power TX in context of Bluetooth Low Energy (BLE) where turn-on times in the microsecond range are achieved [14], [15], [16]. To enable more aggressive duty-cycling with active times in the (sub-) microsecond range, much shorter switching times must be achieved. In a TX, the duty-cycling behavior is largely governed by the PA. It is usually the last active stage in the signal chain, it has large capacitances and quiescent currents that must be switched. Generally, turning on and off PAs is a common concept, but is only rarely studied in detail. [17] and [18] study the turn-on behavior for 40 dBm discrete GaN PAs. References [19] and [20] investigate the effect of duty-cycling integrated PAs on IEEE 802.11 data transmission. Reference [21] reports our initial findings on aggressive duty-cycling behavior of a 400 MHz integrated SiGe PA. In the mmWave region, [22] presents a fully depleted silicon-on-insulator (FD-SOI) PA with fast output toggle specifically for OOK modulation. It utilizes the back-gate bias unique to FD-SOI technology and the energy consumption in sleep state is still 2.5 % of its peak value. In [6], a 7 dBm voltage-controlled oscillator (VCO)-based OOK/pulse amplitude modulation (PAM) TX in FD-SOI is presented that features nearly linear scaling of energy consumption with data rate down to a minimum of 700 nW by means of duty-cycling. Focusing on the switching capability, [23] reports our initial findings on a completely-switchable single-stage SiGe V-band PA.

This article builds upon our previous investigations from [21] and [23] and aims to provide a novel comprehensive top-down study on energy-efficient aggressive duty-cycling, the resulting circuit evaluation and design requirements as well as details on the required fast-switching of integrated mmWave PAs. Focusing on thoroughly assessing the possibilities of aggressive duty cycling, it refrains from downstream investigations at a higher technology readiness level, such as detailed reliability analyses based on process and temperature variations. Beginning with an overview on general aspects of duty-cycling, the requirements for efficient implementation of extreme duty-cycling configurations and their benefits are discussed in section II. The importance of fast switching when targeting minimum latency and high efficiency is highlighted. Subsequently, in section III, focus is narrowed on the related PA characteristics, their measurement and the evaluation of transient waveforms. Moving to circuit design in section IV, the realization of switchable mmWave class-E PAs is studied as they are well suited for energy-efficient aggressive duty-cycling. They generally achieve the highest PAE amongst V-band PAs [8], [24], [25] and are ideal for modulated signals with constant envelope such as GMSK. Although they intrinsically "switch" at RF frequency in steady-state operation, transitions between operational states are not instantaneous. Based on an analysis of the switching behavior and preliminary measurements of a speed-up circuit, a new switchable two-stage SiGe V-band PA is designed and presented in section V to extend our findings of [23] for multi-stage designs with higher output power. The design enables the aggressive duty-cycling discussed earlier and provides an idea on switchable mmWave PAs performance. Measurements of the proposed PA in section VI focus on transient characteristics and especially on duty-cycled data transmission, because there is a lack of reports on this in mmWave literature. Finally, section VII concludes the article.

II. AGGRESSIVE DUTY-CYCLING

Before discussing the advantages and limitations of extreme duty-cycling configurations, the duty-cycling of a transmission system must be reviewed. This is done in two successive stages. First, the transmission is duty-cycled while the TX

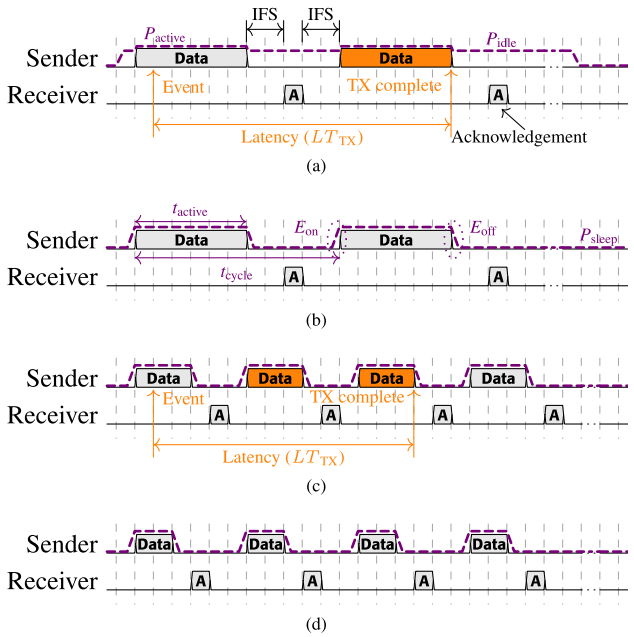

FIGURE 1. Abstracted representation of transmission activity in common wireless communication protocols. The transmitter power consumption is outlined by dashed line. Latency is illustrated for an event generating 6 units of data. (a) Without transmitter duty-cycling. (b) With transmitter duty-cycling. (c) With shortened frame length and IFS. (d) With effective data rate reduced to two thirds.

remains active, then the TX itself is turned on and off accordingly as well.

A. DUTY-CYCLED TRANSMISSION

Many wireless data transmissions are not continuous but duty-cycled. For instance, in time division duplex communication protocols following a carrier sense multiple access with collision avoidance (CSMA/CA) regime like IEEE 802.11 (Wi-Fi) and IEEE 802.15.4 or a similar regime like BLE, data are transmitted in frames [26]. These frames, containing payload data, are always followed by an interframe space (IFS), i.e. a period during which no transmission is allowed. Subsequently, the receiver sends an acknowledgement. In CSMA/CA systems, the next frame may be transmitted after another IFS, sometimes followed by an additional contention window, if the channel is still free. This sequence is sketched in Fig. 1a. When there is a continuous flow of frames, the transmission process can be regarded as duty-cycled. Data are only transmitted during t_{active}, which is a fraction D of one transmission cycle of length t_{cycle}. Then the effective data rate DR_{eff} can be calculated as

$$DR_{eff} = D \cdot DR_{radio} = \frac{t_{active}}{t_{cycle}} \cdot DR_{radio}, \tag{1}$$

where DR_{radio} represents the raw data rate which depends on symbol rate and modulation. The actual information throughput TP is reduced due to non-payload headers included at the start of each frame: A preamble is often necessary for phase and frequency synchronization [27] or gain control at the receiver and further control information may be included. The resulting TP can be calculated as

$$TP = DR_{eff} - \frac{Q_{overhead}}{t_{cycle}}, \tag{2}$$

where $Q_{overhead}$ describes the amount of non-payload data per frame. Besides affecting the TP, duty-cycling also introduces a transmit latency LT_{TX} [2]. Here, it is defined as the delay between data being generated at the sender, e.g. by an external interrupt event, and complete transmission of that data. The duty-cycling configuration must be adjusted to meet any imposed latency requirements.

TABLE 1. Comparison of example duty-cycling scenarios.

Scenario/DR_{eff}	I: Low [a]	II: Medium [b]	III: High [c]
t_{active}	296 µs	1308 µs	53.5 µs
t_{sleep}	380 µs	882 µs	8.7 µs
P_{active}	4 mW	1.22 W	160 mW
P_{sleep}	5.2 nW	462 µW	0 W [d]
Ideal duty-cycling			
$P_{dc,avg} = E_{cycle}/t_{cycle}$	1.75 mW	729 mW	138 mW
Energy savings[e]	56 %	40 %	14 %
Requirements for $\eta_{duty} > 99\,\%$			
Maximum E_{on+off}	12 nJ	16 µJ	87 nJ
Maximum t_{on}/t_{off}[f]	3 µs	13 µs	540 ns

[a] Based on values from [15] and [28]. Only considering TX with 0 dBm output.
[b] Based on values from and [26] and [29]. P_{active} of full system during transmission with 22 dBm. P_{sleep} of full system in light sleep. [c] Based on [30]. Only considering TX with 6 dBm output.
[d] No existing sleep state. Assuming ideal zero consumption.
[e] Compared to continuous consumption of P_{active}.
[f] Assuming dc power during turn-on/off = $P_{active}/2$.

B. DUTY-CYCLED TRANSMITTER

As the TX is only utilized during t_{active}, it can be duty-cycled alongside the transmission as shown in Fig. 1b to reduce energy consumption. By turning off the TX, the required power is reduced from P_{idle} in idle state to P_{sleep} in sleep state. However, switching is not instantaneous and during these turn-on/off periods t_{on}/t_{off} a combined additional energy $E_{on+off} = E_{on} + E_{off}$ is dissipated. The energy E_{cycle} consumed per cycle of length $t_{cycle} = t_{active} + t_{on} + t_{sleep} + t_{off}$ can be calculated as

$$E_{cycle} = P_{active} \cdot t_{active} + P_{sleep} \cdot t_{sleep} + E_{on+off}, \tag{3}$$

where P_{active} is the power in active state and t_{sleep} is the remaining time spent in sleep state. Based on this, [21] introduces the duty-cycling efficiency η_{duty} as

$$\eta_{duty} = \frac{P_{active} t_{active}}{P_{active} t_{active} + P_{sleep} t_{sleep} + E_{on+off}}, \tag{4}$$

which indicates the percentage of energy consumed per cycle that is actually utilized for data transmission independent of η_{active}. This allows evaluating the efficiency of a switching cycle at circuit level and highlights that E_{on+off} and P_{sleep}

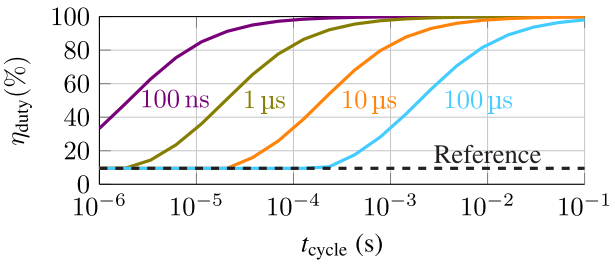

FIGURE 2. Duty-cycling efficiency in scenario I (Table 1) over cycle duration for different $t_{\text{on/off}} = t_{\text{on}} = t_{\text{off}}$. Frame size and thereby t_{active} is adjusted to achieve a constant relative data rate of 5%. Assuming $E_{\text{on+off}} = 2t_{\text{on/off}} \cdot P_{\text{active}}/2$. Lower bound with $t_{\text{on/off}} = \infty$ is shown for reference.

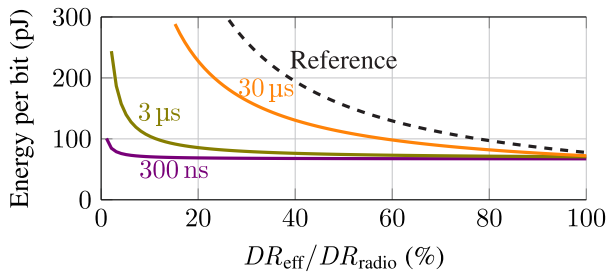

FIGURE 3. Energy per bit in scenario III (Table 1) over relative data rate for different $t_{\text{on/off}} = t_{\text{on}} = t_{\text{off}}$. Data rate is reduced by reducing frame size and thereby t_{active}, but transmitting in the same interval. Assuming $E_{\text{on+off}} = 2\,t_{\text{on/off}} \cdot P_{\text{active}}/2$. Energy per bit without duty-cycling (continuous P_{active}) is shown for reference.

must be minimized. While P_{sleep} is reduced by minimizing leakage [14], [15], $E_{\text{on+off}}$ is best reduced by shortening the switching times t_{on} and t_{off}. The desired dimensions of these depend on the application scenario and active state characteristics.

To illustrate the order of magnitude and for further reference below, three scenarios based on specifications derived from state-of-the-art circuits and protocols are presented in Table 1 together with requirements to implement energy-efficient duty-cycling ($\eta_{\text{duty}} > 99\,\%$). All scenarios assume a continuous frame-based transmission without collisions. Scenario I represents a low power, low data rate application with a continuous BLE transmission based on circuit parameters from [15] and protocol timing from [28]. Scenario II describes a medium data rate application. It represents a continuous IEEE 802.11b transmission with 11Mbps based on commercial hardware [29] and protocol timing and minimum contention window duration from [26]. Finally, scenario III describes a short-range and high-speed 60 GHz link based on [30].

C. AGGRESSIVE DUTY-CYCLING

In a duty-cycled communication, t_{cycle} should be as short as efficiently possible to reduce latency: Reducing t_{cycle} and consequently frame duration (corresponding to t_{active}) and IFS duration as shown in Fig. 1c reduces the worst-case LT_{TX} compared to Fig. 1a at the same DR_{eff}. This also applies when data generated by a singular event is split across multiple frames due to the smaller individual payload. Generally, this can be seen as downscaling of a CSMA/CA regime on the time axis and must be supported by all network devices. Furthermore, to maintain a constant LT_{TX}, t_{cycle} should not increase at lower data rate. To nonetheless adapt the average dc energy consumption $P_{\text{dc,avg}} = E_{\text{cycle}}/t_{\text{cycle}}$ to the required data-rate, it is necessary to reduce frame duration and therefore t_{active} as shown in Fig. 1d instead of increasing the time between frames. If a low LT_{TX} is desired, this results in a very short t_{active} at low DR_{eff}.

The shorter t_{active} is, the more "aggressive" the duty-cycling becomes and the more important efficient and fast switching behavior gets. It is necessary to reduce the overhead both in terms of data (Q_{overhead}) and in terms of energy ($E_{\text{on+off}}$) to avoid decreasing TP and η_{duty}, respectively. Reducing Q_{overhead} must be done at protocol level and may complicate synchronization or transmission of control data. However, due to the shorter t_{cycle} there is less time between frames which potentially reduces the required information per frame. Alternatively, [27] proposes a method to replace the synchronization preamble entirely. Focusing on the TX hardware, a sufficiently low $t_{\text{on}}/t_{\text{off}}$ is necessary to maintain a high efficiency of the TX even at low t_{cycle} as shown in Fig. 2 based on scenario I. Similarly, to achieve $P_{\text{dc,avg}} \propto DR_{\text{eff}}$, $E_{\text{on+off}}$ and by extension $t_{\text{on}}/t_{\text{off}}$ must be minimal. This is highlighted in Fig. 3 based on scenario III. Only for a $t_{\text{on}}/t_{\text{off}}$ of 300 ns, an approximately constant energy per bit is achieved even at low data rates.

III. GENERAL ASSESSMENT OF SWITCHABLE PAS

In order to study the turn-on and turn-off behavior and evaluate (3) for a duty-cycled PA, it is essential to define active and sleep state and discuss assessment thereof.

A. KEY CHARACTERISTICS

In sleep state, only the instantaneous energy consumption P_{dc} is of interest. Once it is below a certain threshold near P_{sleep}, the PA can be considered sleeping. The active state on the other hand is crucial for functionality. Here, the requirements heavily depend on the system and application. In general, a PA should provide a required amplification. Therefore, the primary generic measurable active state characteristic is the output power for a given input power level. The amplifier can be considered active once the output power has settled within a certain relative range $\pm p$ of the continuous-wave (CW) value. For amplifying modulated signals, it is additionally necessary to wait until relevant metrics regarding linearity and distortion have exceeded or fallen below a certain threshold, depending on the individual application. Alternatively, a more holistic metric can be used in systems with digital modulation schemes. The error vector magnitude (EVM) quantifies errors in the constellation diagram of the baseband signal after ideally down-mixing the output RF-signal, and therefore captures all distortions relevant for data

transmission. For reliable demodulation, EVM should be below a certain threshold defined on system level.

The timespans t_{on} and t_{off} describe the delay from toggling the enable signal until the respective state is reached based on the above definitions. Since the active state is more crucial for data transmission and reaching it usually takes longer due to the more demanding requirements, t_{on} is studied more extensively. From an efficiency point of view, E_{on+off} consumed during t_{on} and t_{off}, here representing the energy wasted in one switching cycle, is most important.

B. EXPERIMENTAL EVALUATION

Determining these timings is challenging in simulation and measurement. The frequency-domain description obtained from EM-simulation of passive elements, which are crucial for accurately describing the behavior of a mmWave-circuit, complicates transient simulations. The necessary convolution and other parts of the simulator have been focus of continued investigation [31], [32]. Nonetheless, very careful setup of simulator options and testbenches is still necessary and convergence problems are frequent.

Measurements are challenging due to the short transients. To analyze the output signal and determine t_{on}/t_{off}, either a spectrum analyzer in zero-span mode, a signal analyzer with amplitude demodulation or a real-time oscilloscope (RTO) can be used. To observe rise times in the (sub-) nanosecond range, gigahertz of bandwidth are necessary. Additionally, to quantify delays and record control signals, simultaneous measurement of further signals is obligatory. Hence, an RTO with sufficiently high sampling rate and bandwidth to capture the fundamental frequency is most versatile, especially when combined with a vector signal analyzer (VSA) software for per-symbol EVM calculation. If no suitable RTO is available, the output signal must be mixed to an intermediate frequency first, but additional de-embedding is necessary to remove the introduced delays. To determine t_{on} based on output power settling, a single-tone CW is supplied to the PA, and the time until the derived output power has settled within $\pm p$ is measured. Alternatively, to assess t_{on} based on an EVM definition, a modulated signal is supplied to the PA either by a vector signal generator or an arbitrary waveform generator (AWG). The output waveform is demodulated and analyzed per symbol with a VSA software on a signal analyzer or an RTO. Sufficient transmission cycles have to be acquired to determine the number of symbols and the according t_{on} after which the EVM is reliably below the defined threshold. Measuring t_{off} directly based on the P_{dc} threshold is usually not possible, because P_{dc} cannot be probed in real-time due to on-chip capacitance on the supply net. An alternative is to study the fall-time of the PA output as it is expected to closely correlate with t_{off}. To determine E_{on+off}, the energy consumed per cycle is compared to the energy consumed during the phase the PA is considered active. For this, after obtaining P_{active} with CW, the PA is duty-cycled, $P_{dc,avg}$ is measured and the time t_{active} is extracted from the output power curve.

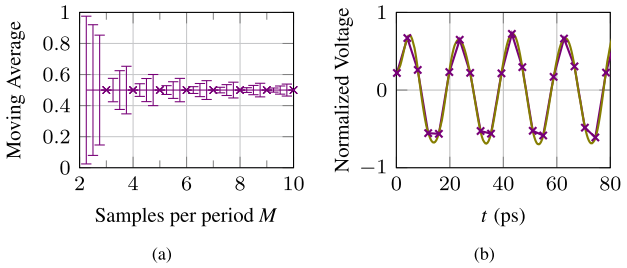

FIGURE 4. (a) Discrete moving average of $\sin^2$ over one period for different samples per period M and error range due to integer filter length ($\lfloor M \rfloor$). (b) Oversampling of measured samples with $O_s = M = 50$.

When neglecting P_{sleep}, E_{on+off} can then be estimated as [23]

$$E_{on+off} = t_{cycle} P_{dc,avg} - t_{active} P_{active}. \tag{5}$$

For any evaluations based on the output power curve, prior processing is necessary to extract the signal power at the fundamental frequency f_c from a sampled time-domain RF-signal acquired by an RTO with sampling frequency f_s or in simulations. It represents the instantaneous output voltage, may include harmonics generated by the PA, if not filtered by the anti-aliasing filter of the RTO, and waveform peaks may not be captured due to the limited oversampling $O_s = \frac{f_s}{f_c}$ possible at mmWave. To reliably determine the transient behavior of the PA output nonetheless, we propose the following procedure briefly introduced in [23] based on the time-discrete waveform sampled above Nyquist frequency ($O_s > 2$): A bandpass filter with bandwidth B_{BP} around f_c is applied to extract the fundamental signal. Subsequently, the signal is converted to an instantaneous power curve considering the load impedance and the desired signal power curve is calculated by a moving average with duration of one period ($1/f_c$). Finally, a lowpass filter is applied to remove noise introduced by measurement and sampling. If O_s is low and non-integer, the result of the discrete moving average can vary depending on the number of sampling points per period as shown in Fig. 4a. Therefore, the measured waveform should be first resampled to an integer O_s, ideally a high value of e.g. 50, using the Fourier method. This minimizes calculation errors and restores the full sinusoidal form for better visual analysis as shown in Fig. 4b.

The bandpass and lowpass filtering steps generally introduce not only a phase shift but also limit the rise time of the signal. Here, second-order Butterworth filters are used as they have no phase delay at center frequency or dc, respectively, have a flat frequency response and exhibit a reasonably fast rise time: As derived in the appendix, the bandpass has an envelope step response $a(t)$ described by

$$a(t) = 1 - \cos\left(-\frac{1}{4}\pi + \frac{\sqrt{2}\omega_c t}{4Q}\right)\sqrt{2}e^{\left(-\frac{\sqrt{2}\omega_c t}{4Q}\right)}, \tag{6}$$

which reflects the distortion the envelope of a stepped sine at f_c experiences. Its settling time is inversely proportional to B_{BP}: For example, the distortion is less than 1 % after

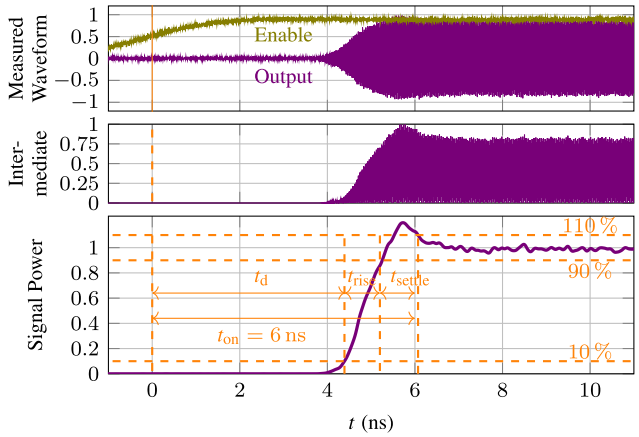

FIGURE 5. Exemplary analysis of signal generator rising output: Acquired voltage waveforms, intermediate instantaneous power curve after bandpass filtering and resulting signal power. Amplitudes are normalized to peak or final value.

$T_{d,BP} = \frac{0.968}{B_{BP}}$ based on (13). Hence, a sufficiently large B_{BP} must be chosen to ensure $T_{d,BP}$ is much smaller than the expected signal rise time. In the following, $Q = \frac{f_c}{B_{BP}} = 5$ is used.

In Fig. 5, the turn-on behavior of a lab signal generator with pulse modulation is evaluated with $p = 10\,\%$. It can be divided into three externally observable phases: A delay t_d after the EN signal is switched, an initial rise time t_{rise} of the output power envelope up to 90 % and a settling time t_{settle} until the output power has settled within $\pm 10\,\%$. This leads to a combined

$$t_{on} = t_d + t_{rise} + t_{settle}. \tag{7}$$

IV. DESIGN OF SWITCHABLE MMWAVE CLASS-E PAS

Mainly two intrinsic sources of delay are responsible for the externally observable t_{on} in duty-cycled operation of mmWave class-E PAs: OPS and the rise of the signal swing in the load network.

A. LOAD NETWORK RISE TIME

Duty-cycling the transmission as described in section II-A means duty-cycling the carrier signal, i.e. the input signal to the PA. Regardless of any OPS, the load network has a lowpass effect on this signal power. In steady-state class-E operation, a non-negligible amount of energy circulates in the network due to one or more internal resonant circuits. Once an input signal is applied, this oscillation energy slowly builds up until the steady-state output power is reached after a timespan $t_{rise,load}$. Based on an ideal 60 GHz switching PA shown in Fig. 6a, this behavior is investigated for different load networks. Fig. 6b shows the output rise behavior with a classic shunt-C/series-tuned class-E load and Table 2 compares $t_{rise,load}$ across different ideal load networks. As long as a low-inductive supply connection is present, the output rises in less than 20 fundamental periods.

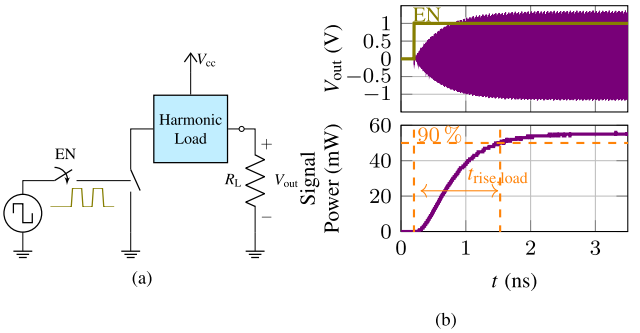

FIGURE 6. (a) Switching amplifier with ideal switch and load network and (b) its output rise behavior with shunt-C/series tuned class-E load with 10 nH dc-feed.

TABLE 2. Comparison of output power rise time for Fig. 6 with different harmonic loads.

Harmonic load (dimensioned according to reference)	$t_{rise,load}$ (ps)
shunt-C/series-tuned with 10 nH dc-feed L [33]	1329
shunt-C/series-tuned with 400 pH dc-feed L [34]	248
shunt-C/series-tuned with 200 pH dc-feed L [34]	205
series-L/parallel-tuned [33]	123
doubly tuned transformer [24]	282
transmission-line based [35]	120

B. OPERATING POINT SWITCHING

To also duty-cycle the transmitter section II-B and in particular the PA, it is necessary in a real PA to switch the transistor operating point between sleep and active bias. Unlike low-frequency class-E PAs which can be driven by a high-impedance square-wave voltage waveform [21], mmWave class-E PAs are usually driven by a dc-decoupled near sinusoidal waveform. To still accomplish "switch-like" behavior of a SiGe transistor, it is biased in active region [24], [36], [37] with a resulting quiescent current flowing, and sufficient drive power is necessary to alternate between saturation and cut-off region. Some designs can also be biased just below the cut-in threshold [25], but a leakage current with noticeable effect on P_{sleep} is still expected to flow. Generally, the exact bias level affects the switch duty-cycle, i.e. the percentage of an RF-signal period the switch is conducting. The switch duty-cycle is an aspect in CW-design [38] and different from the PA duty-cycle described in this article. To minimize P_{sleep}, the transistor should be fully turned off in sleep state to remove any quiescent current. Therefore, it is necessary to reduce either the collector or the base bias to near zero.

Since the collector bias current is inherently larger than the base bias current, turning on and off the collector bias requires much larger switch devices with an equal rise in capacitance which leads to longer switching times and higher switching losses. Nonetheless, it can be attractive to control the collector bias and this is frequently done for envelope tracking (ET). By regulating the supply voltage to track the envelope of the baseband signal, a class-E PA can be efficiently operated with non-constant envelope signals [39] or the efficiency

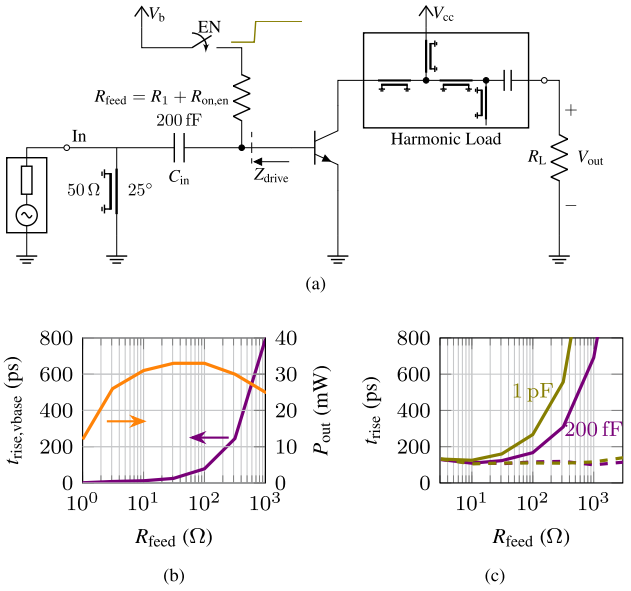

FIGURE 7. (a) Class-E PA stage with base bias switch. (b) Base voltage rise time $t_{rise,vbase}$ and CW output power P_{out} vs. R_{feed} with $C_{in} = 200$ fF. (c) PA output t_{rise} with input signal present for different C_{in} and without (solid) and with (dashed) temporarily shorting base to V_{cc}.

of a linear PA can be significantly increased [40]. The regulators required for this can achieve voltage transition from minimum to maximum in the range of 200 ns [41], but are usually not designed for turning off the PA completely. Moreover, they are complex systems and require noticeable chip area [40], [41]. Much simpler and faster switching can be achieved by reducing the base bias to zero. Besides the lower required current handling capability, this is further simplified by the resistive base bias commonly used in PAs designs [24], [42]. Consequently, an on-resistance $R_{on,en}$ of a base bias switch is less problematic and an additional RF-bypass capacitance after the switch is not needed. Hence, base bias switching is favored here, but could be combined with ET.

To provide the desired amplification after turning on, the bias level and respective operating point has to be reached again. Based on the PA stage shown in Fig. 7a with transmission-line based load, the base charge behavior is analyzed. The voltage rise time of the base node $t_{rise,vbase}$ is dominated by the RC-element formed by R_{feed} and the combined capacitance at the base node. The capacitance is primarily determined by the CW-design, but a minimum series matching/dc-block capacitor is preferable and crucial for fast turn-on. Similarly, R_{feed} should be minimal as $t_{rise,vbase} \propto R_{feed}$. However, it also affects the CW-performance as shown in Fig. 7b: If too small, the drive impedance Z_{drive} seen by the transistor is affected. If too large, the bias point is shifted. The resistor R_1 should be chosen to attain the minimum R_{feed} viable from CW-perspective. Besides improved transient behavior, a low impedance base feed is also beneficial for beyond BV_{CEO} operation [25].

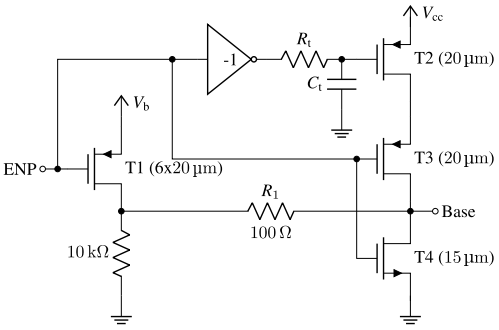

FIGURE 8. Kick-starter schematic based on [23] with transistor width.

C. KICK-STARTER CIRCUIT

Intuitively, the two phases are executed in sequence: The input signal is only applied after the stable operating point has been reached. Then the charging of the base node for OPS contributes to t_d and the large-signal rise in the load network to t_{rise}. However, in practice both can be performed partially simultaneously, leading to an increased t_{rise} but minimal t_d and lower total energy consumption. For the PA shown in Fig. 7a, t_{rise} is dominated by the load network. However, the delay due to switching the base node can become significant when a large C_{in} or a large R_{feed} is required from CW-design. This can be circumvented by bypassing R_1 for a short time when turning on the PA to quickly charge the capacitances via a low-ohmic path [23]. Thereby, t_{rise} remains minimal regardless of C_{in} and R_{feed} as shown in Fig. 7c.

The proposed base charge procedure is implemented by the circuit labeled kick-starter briefly introduced in our earlier work [23] and shown in Fig. 8. A large transistor T1 acts as a low-ohmic but slow bias switch for steady-state operation. Narrower transistors T2 and T3 with a lower input capacitance, combined with the simple CMOS inverter, temporarily bypass T1 and establish a low-ohmic path between V_{cc} and the base node for a short time t_{kick}. The time is tuned depending on the base node capacitance and should be low enough to avoid overswing of the base voltage. It is controlled by the capacitance C_t, partially realized by the parasitic capacitances at the node, and the resistance R_t, partially realized by the output resistance of the inverter. Simulations of the final circuit realization described in section V show a variation of t_{kick} of around 10 % across temperature and process corners. If it is larger than necessary, the base voltage may temporarily exceed the desired value, but no reliability issues are expected [43]. For the turn-off process, T4 ensures the base node is quickly discharged to achieve a fast t_{off}.

For preliminary experimental evaluation, a trial PA with a separate kick-starter supply pad is fabricated. The measured turn-on behavior is shown in Fig. 9. A settling behavior not visible in simulations becomes evident. It may be caused by reflections at the ENP input or by thermal settling behavior. Furthermore, a temporary output power drop after the initial rise is present. Apparently, the kick-starter already turns off

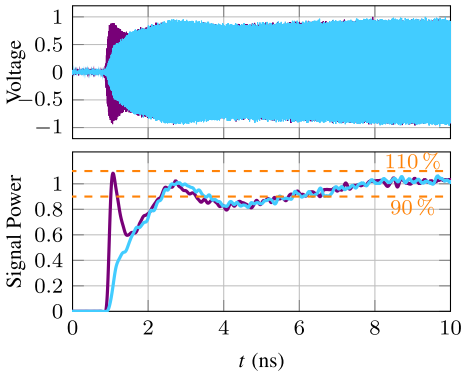

FIGURE 9. Preliminary measurement of trial PA. Normalized measured output voltage and derived signal power with (purple) and without (blue) kick-starter.

again before T1 is fully enabled, resulting in a temporary output power drop. Hence, depending on the specifications, the total t_{on} is dominated by t_{settle}. However, the kick-starter indeed results in a much faster initial t_{rise} of just 100 ps instead of 1.5 ns. The current drawn by the kick-starter circuitry is negligible both in always-on mode as well as in duty-cycled mode. Even at $t_{cycle} = 40$ ns it is lower than the base bias currents. Therefore, the circuit can improve t_{rise} at little cost but needs tuning of its timing to remove the undesired output power drop.

V. IMPLEMENTATION

To enable efficient aggressive duty-cycling as presented in section II, a PA with ultra-fast $t_{on/off}$ and low E_{on+off} is required. Based on the presented scenarios, a $t_{on/off} < 1$ µs and E_{on+off} in the nanojoule range is desired. An output power around 15 dBm is selected to achieve a reasonable communication distance and a large-signal gain $>$ 10 dB is necessary to ease requirements on the preceding stages. For this, we propose the PA shown in Fig. 10 based on the switching considerations in section IV. It is implemented in IHP SG13G2 BiCMOS technology with copper back end of line. Two class-E stages are necessary to attain the desired large-signal gain. The transistors are dimensioned as a tradeoff between current handling capability, output capacitance and required input drive power. The harmonic load and output matching network of the main stage based on grounded coplanar waveguide (G-CPW) is derived from [35]. It implements the collector dc-feed, matches the optimum load impedance to a 50 Ω load and presents an open-circuit to the second and third harmonic at Z_{load} plane. From the fast-settling networks listed in Table 2, it is the most suitable for this design. It can still exhibit the desired class-E behavior with the transistor output capacitance at the chosen device size. For higher capacitance or at higher mmWave frequencies, at which the impact of the capacitance is greater, the doubly tuned transformer network would be more suitable [24]. In contrast, the series-L/parallel-tuned inverse class-E harmonic network used in [23] is more affected by the capacitance and already unsuitable at V-band here. Generally, inductor-based networks further suffer from the necessary minimum conductor width calculated considering the estimated currents and based on the maximum current density for the top-metal layers. However, the minimum width also limits the maximum impedance that can be achieved for G-CPW in the proposed load network to around 50 Ω. For these G-CPW, the upper thick copper layer of the technology is used despite the top aluminum layer generally providing a better transmission line performance due to the higher substrate separation [44]. Stability of the circuit design is studied using the k-factor of simulated large-signal S-parameters as well as the Othomo method based on harmonic balance simulations implemented in *Keysight ADS* [45]. Due to stability concerns around 30 GHz, a half harmonic trap [25] is added at the input of each stage.

To achieve an output power of up to 15 dBm, a supply voltage of $V_{cc} = 1.7$ V is necessary. Based on class-E theory, a theoretical voltage swing of up to $3.56V_{cc} = 6$ V [25] is calculated, but simulations show that the collector voltage does not exceed 3 V as seen in Fig. 11. Although this is still higher than the specified BV_{CEO} of the used technology, it is not necessary to stack transistors for the core switch. At this frequency, self-heating of the transistor can no longer follow the dynamic signal swing allowing a higher collector-emitter voltage without reducing performance or reliability [43]. Additionally, a low-ohmic bias feed reduces the impact of the avalanche effect [25]. From Fig. 11 is also visible that zero voltage switching, characteristic to ideal class-E operation, is not fully realized. At mmWave, PAs generally only achieve class-E-like behavior due to lack of square-wave drive signals and high parasitics [24], [25], [46].

Finally, the kick-starter circuit described in section IV-C is introduced to implement OPS functionality. It is realized with the available CMOS devices in the BiCMOS process. The kick-starter supply voltage should be identical to that of the digital circuit which provides the enable signal. To reduce pad count, $V_{cc,driv}$ is re-used. Both class-E stages are controlled by a separate circuit fine-tuned for the respective stage. Although the larger second stage has a larger idle power, the first stage still has non-negligible contributions and should be turned-off as well. Both stages are turned on simultaneously here. If t_d was large, a staggered scheme would be preferable for efficiency, but here t_{rise} and t_{settle} are expected to dominate. From transient simulations, the turn-on time is not noticeable larger compared to only switching the second stage. The simulated turn-on behavior of the complete PA core excluding pads based on electro-magnetic (EM)-simulated blocks is shown in Fig. 12 and $t_d = 350$ ps and $t_{rise} = 400$ ps are derived.

To provide stable bias voltages and present low-ohmic RF-shorts to the switching and matching networks, zero-ohm lines [47] are used to connect the circuit core with the pads. To maintain the integrity of the control signal when probing and measuring the circuit, it is terminated with 50 Ω at the core by a parallel 100 Ω resistor at both stages. Driving it up

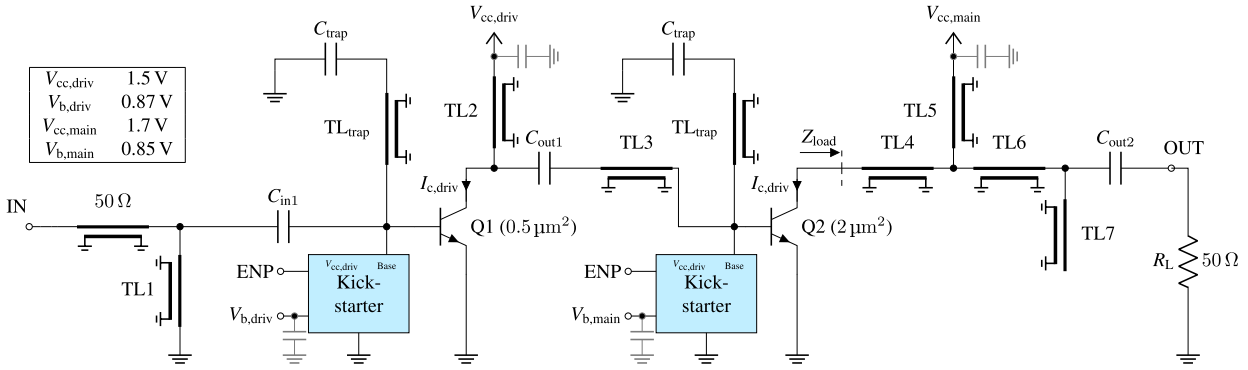

FIGURE 10. Top level schematic of proposed two stage class-E amplifier.

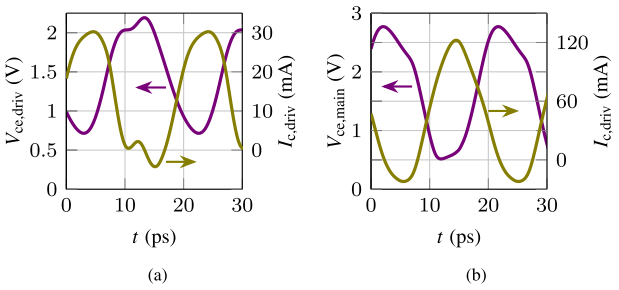

FIGURE 11. Simulated waveforms at switch transistors of (a) driver stage and (b) main stage considering layout parasitics. $I_{c,driv}/I_{c,driv}$ include current flowing into (parasitic) collector capacitances.

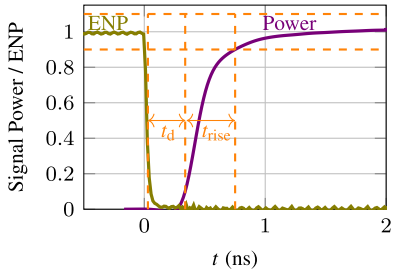

FIGURE 12. Simulated normalized signal power rise behavior at 51 GHz. t_{rise} is nearly identical between 48 GHz to 55 GHz.

to 1.5 V results in non-negligible power dissipation in this test setup. If the PA is integrated with digital control on the same chip, the costly 50 Ω termination is not necessary. All signals are connected to GSG-pads using 50 Ω lines.

VI. MEASUREMENT

To prove and evaluate the aforementioned concepts by measurements, a chip was fabricated and experimentally characterized on-wafer in a laboratory. The chip shown in Fig. 13 occupies 0.8 mm^2 with pads. Data transmission measurements are performed based on GMSK and O-QPSK (using half-sine pulse shaping) with constant envelope and with $\frac{\pi}{4}$-DQPSK with 2.9 dB peak-to-average power ratio (PAPR) due to RRC pulse shaping. As no specific application is focused, $p = 10\,\%$ for output power settling and a peak

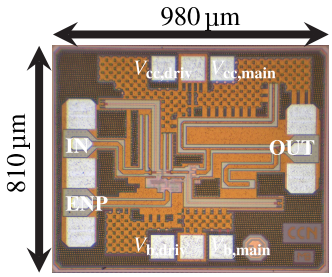

FIGURE 13. Die photograph.

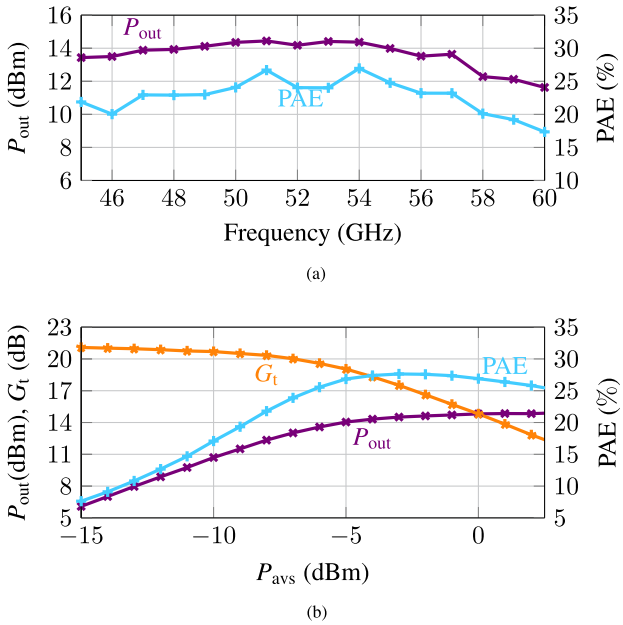

FIGURE 14. Large-signal characteristics (a) vs. frequency f for $P_{avs} = -2$ dBm and (b) vs. available source power P_{avs} at $f = 51$ GHz.

EVM threshold of 15 % for modulation quality is chosen. For the tested modulations, usually a root-mean-square (RMS) EVM in the range 10 % to 30 % is specified [9], [11].

A. CONTINUOUS-WAVE CHARACTERISTICS

The CW behavior is investigated using a signal generator and a power meter. Cable and probe losses at the input are pre-compensated in the signal generator, with output losses

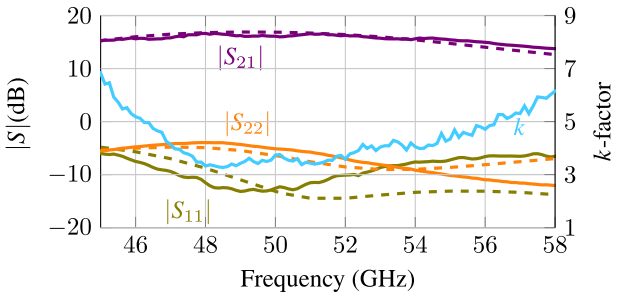

FIGURE 15. Measured (solid) and simulated (dashed) S-parameter at $P_{avs} = -2$ dBm.

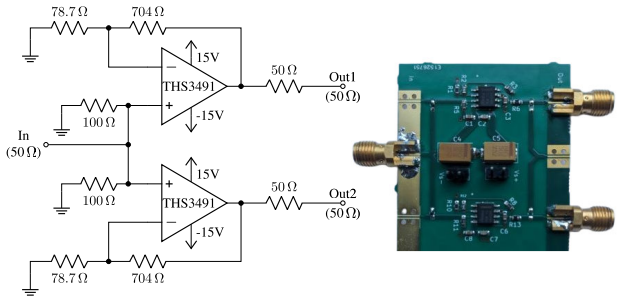

FIGURE 16. Broadband amplifier for enable signal.

de-embedded after measurement. A spectrum analyzer is used to check for undesired frequency components. Fig. 14 shows the output power P_{out} and the PAE over frequency for an available source power of $P_{avs} = -2$ dBm. An output power around 14 dBm at a PAE around 25 % is provided from 48 GHz to 55 GHz. In Fig. 14a, P_{avs} is swept at 51 GHz. A peak small-signal gain of 21 dB is measured, while the gain at maximum PAE of 27 % is 17 dB. The S-parameters shown in Fig. 14b are obtained using a vector network analyzer with a *RFLambda* PA in its source path to achieve $P_{avs} = -2$ dBm. If the PA is turned off by a high ENP control, $V_{cc,driv}$ supplies the kick-starter circuitry, while $V_{cc,main}$ is only loaded with the leakage of the second stage core transistor. At room temperature, 11.5 nA and 0.5 nA are drawn from $V_{cc,driv}$ and $V_{cc,main}$, respectively, regardless of P_{avs}. With negligible currents drawn from the base bias voltage supplies, this results in a total sleep consumption of $P_{sleep} = 18.1$ nW compared to $P_{idle} = 46$ mW when not turning off the PA.

B. DUTY-CYCLING CHARACTERISTICS

Below, the measurement setup for duty-cycled measurements and the obtained single-tone and data transmission results are detailed.

1) MEASUREMENT SETUP

To be able to precisely measure turn-on/off times in the order of a few nanoseconds, a fast-rise enable signal is required. For this an AWG with 256 GSa s^{-1} and 70 GHz of analog bandwidth is used to generate the control signal. To drive the 50 Ω ENP input of the PA up to the required 1.3 V, a discrete broadband control signal amplifier shown in Fig. 16

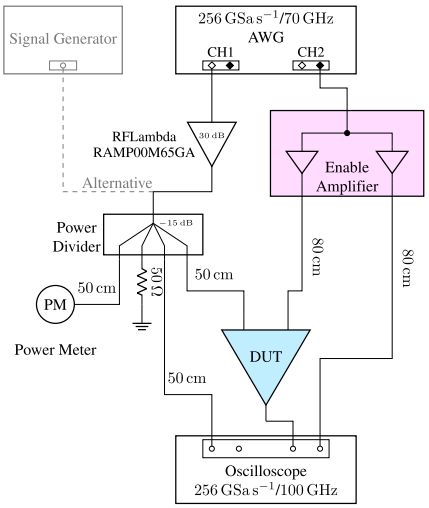

FIGURE 17. Transient measurement setup.

TABLE 3. Measured EVM in duty-cycled mode vs always-on.

Modulation		GMSK	O-QPSK [a]	$\frac{\pi}{4}$-DQPSK [b]
P_{avs} [c] (dBm)		−2	−2	−10
$P_{dc,avg}$ (mW)	Duty-cycled	9.3	9.3	6
	Always-on	54	54	50
EVM (%)	Reference	3.8	4	4.8
EVM (%)	Duty-cycled	5.8	4.6	7.2
	Always-on	4	4	6.8

[a] with half-sine pulse-shaping [11] [b] with RRC pulse-shaping [9]
[c] average over transmission

is built based on commercial components. Combined with compensations on the AWG, an ENP rise time of 1 ns is accomplished. The complete measurement setup is shown in Fig. 17. The device-under-test (DUT) RF input is excited by a signal generator with a single-tone signal or the AWG combined with a broadband preamplifier is used instead to generate modulated signals for data transmission tests. A real-time oscilloscope with 256 GSa s^{-1} is used to capture the PA output waveform as well as a duplicate of ENP for reference. Furthermore, the input signal is split by a four-way power divider to confirm the power level at the input and to simultaneously capture the input transient. The output cable delay skew is determined by measurement of a through structure and corrected on the RTO. Unless otherwise noted, all reported measurements are carried out with a 51 GHz (carrier) signal and the PA is operated at its efficiency peak with an input power of −2 dBm for constant envelope signals and with an average input power of −4 dBm for $\frac{\pi}{4}$-DQPSK. Measurements have been repeated at different frequencies, but similar duty-cycling characteristics are observed across the tested range from 48 GHz to 55 GHz.

2) SINGLE-TONE

To measure turn-on/off behavior based on the output power, the PA is duty-cycled and the input is excited with a CW signal. The obtained waveforms are processed as described

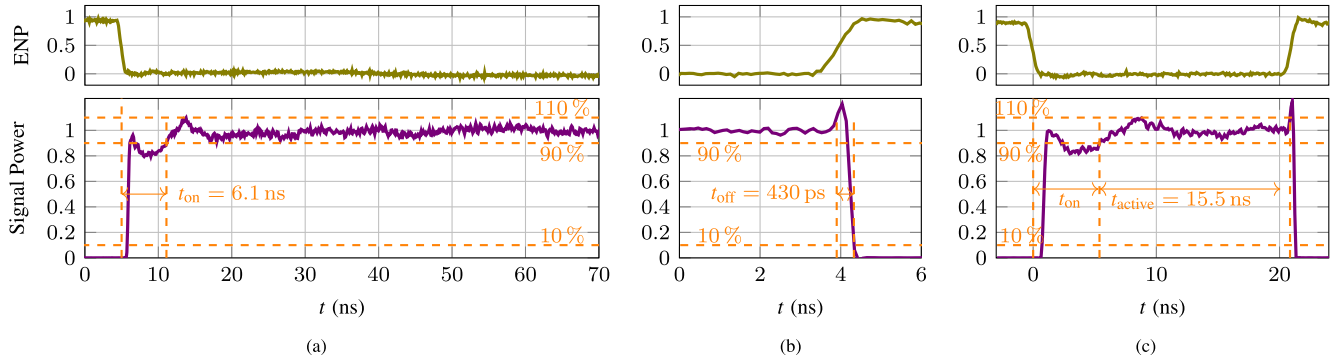

FIGURE 18. Normalized enable signal and signal power derived from measured output waveform for: (a) turn-on, (b) turn-off and (c) duty-cycled operation with timespan t_{active} effectively usable for data-transmission.

TABLE 4. Comparison with state-of-the-art integrated V-band SiGe power amplifiers.

	Freq. (GHz)	V_{cc} (V)	P_{out} (dBm) [a]	G_t (dB) [a]	PAE_{max} (%)	t_{on} (ns)	E_{on+off} (pJ)	P_{sleep} (nW)	Comment
[42] 2012	60	3.3	15[b]	9.5[b]	29	-	-	-	cascode, class-AB
[25] 2014	41	2.5	20[b]	10[b]	31.5	-	-	-	class-E
[48] 2019	61.5	3	14[b]	9.5[b]	11	-	-	-	cascode, class-A
[24] 2022	63	2	16[b]	7[b]	35	-	-	-	class-E, balanced
[23] 2023	54	1.2	8.5	6.5	25	7.3 [c]	≈ 100	2.82	class-E^{-1}
[49] 2024	66	2.5	11	11	11	-	-	-	cascode, class-A
[50] 2024	43	3.3	24	21[b]	35	-	-	-	cascode, class-AB
This work	51	1.7	14	17	27	6.1 [d]	< 800	18.1	class-E

[a] At maximum PAE [b] Estimated from graph [c] Time from 5 % P_{out} until settled within 100 ± 5 % of CW-value [d] Time from enable signal toggle until P_{out} settled within 100 ± 10 % of CW-value

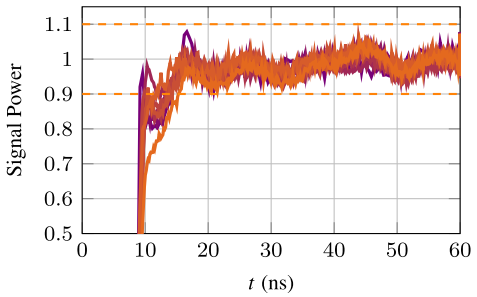

FIGURE 19. Comparison of derived signal power curve at turn on measured at different frequencies and duty-cycling configurations.

in section III-B and shown in Fig. 18. A $t_d = 750$ ps, related to the ENP mid-level crossing, and a $t_{rise} = 350$ ps, similar to simulations, are derived. The undesired initial output power drop has been reduced compared to preliminary measurements, but t_{settle} still dominates the turn-on process in measurements. This leads to a total $t_{on} = t_d + t_{rise} + t_{settle}$ of the PA with $p = 10$ % (−0.46 dB to 0.41 dB) of 6.1 ns. This settling behavior varies slightly across different frequencies and different duty-cycling configurations as shown in Fig. 19. However, generally t_{on} remains around 6 ns. In some scenarios, the derived signal power waveforms contain peaks within the first 100 ns that exceed the p boundary again for a sub-nanosecond duration. It is unclear whether this is actually present on the output waveform or only introduced in measurement and processing.

When measuring the turn-off behavior, a fall time of the RF-signal of 430 ps is observed. E_{on+off} is determined as described in section III-B. It is dominated by the settling phase as shown in Fig. 18c and highly sensitive to the exact active state definition. The stricter the requirement, the more energy is wasted before reaching it. Based on the $T = 10$ % passband, E_{on+off} is smaller than 800 pJ over measurements with different t_{cycle} and D.

3) DATA TRANSMISSION

To confirm the duty-cycled data transmission performance, the PA is tested with GMSK, O-QPSK and $\frac{\pi}{4}$-DQPSK signals. A symbol rate of 1 GBaud is used to utilize the high available bandwidth and highlight the high data rate. The timings are adjusted so that input transmission burst and the enable signal are aligned at the probe tip. A VSA application on the oscilloscope detects the transmission bursts, demodulates the signal and calculates the EVM per symbol. In Fig. 20, the analysis of the demodulated output signal is shown for a GMSK input signal with $t_{cycle} = 1$ µs and $D = 10$ % resulting in 100 symbols per cycle. The first symbol of the burst is not properly generated and distorted even for the reference waveform. For the PA output, the EVM is below 15 % starting with the third symbol. Turning on the enable signal t_{pre} before the data signal does not improve this behavior. Similar results are obtained for the other modulations. In Table 3, the total RMS EVM neglecting the first two symbols is compared between duty-cycled mode

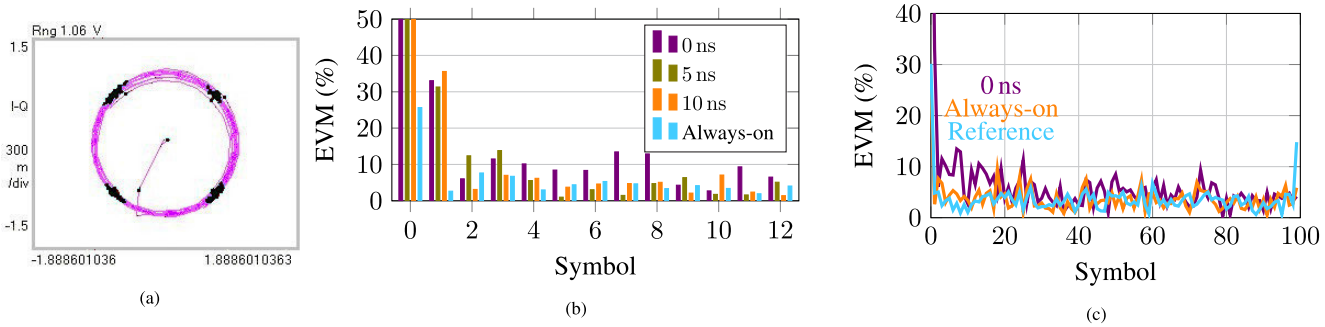

FIGURE 20. Signal quality analysis of 100 symbol/100 ns pulse in duty-cycled 1 GBaud GMSK transmission: (a) Demodulated constellation diagram. (b) EVM of the first transmitted symbols for different advance turn-on of the enable signal t_{pre}. (c) EVM over the entire pulse comparing duty-cycled and always-on operation with reference path.

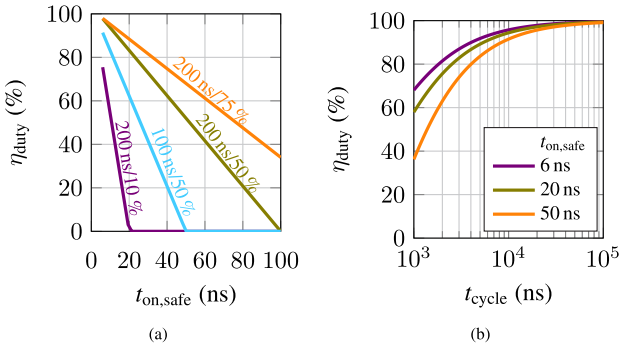

FIGURE 21. (a) Duty-cycling efficiency vs turn-on safeguard period for measurements with different values of t_{cycle} and D. (b) Duty-cycling efficiency vs cycle duration for different turn-on safeguard with $D = 10\%$.

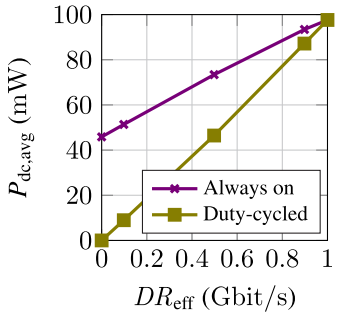

FIGURE 22. Measured $P_{dc,avg}$ over effective data rate using duty-cycled 1 Gbaud GMSK modulation with $t_{cycle} = 1\ \mu s$. The first two symbols of each transmission are ignored to achieve an RMS EVM better than 6%.

and always-on mode. Turning on the PA just in time for the transmission only slightly deteriorates signal quality. The measured EVM values are well below the defined limits even in duty-cycled mode.

C. EVALUATION

In Table 4, the measured characteristics are summarized and compared with the state of the art. Comparable performance is achieved in terms of CW operation. Focusing on duty-cycling behavior, it becomes clear that the respective efficiency highly depends on the active state requirements.

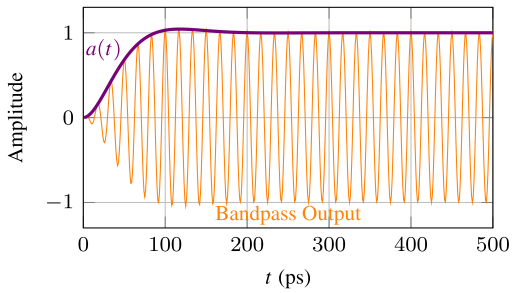

FIGURE 23. 2nd order Butterworth bandpass filter response to a stepped sine input and its envelope based on (11).

Depending on the application this PA is used in, it is necessary to wait for a safeguard period $t_{on,safe} \geq \max(t_{on})$ to ensure the PA has settled regardless of frequency and other influence quantities. For digitally modulated data transmissions, this can also be implemented by discarding the first symbols of each cycle at receiver side. At very low t_{cycle} and D, $t_{on,safe}$ can drastically reduce η_{duty} as shown in Fig. 22a. However, even at for example $D = 10\,\%$, duty-cycling remains efficient for $t_{cycle} > 10\,\mu s$ as shown in Fig. 22b. When less sensitive modulation is used, only a short $t_{on,safe}$ is necessary. For the tested 1 GBaud modulations, symbols can be successfully transmitted after 2 ns which can partly be attributed to the kick-starter circuitry reducing t_{rise}. Therefore, the power consumption in duty-cycled mode scales linearly with effective data rate down to almost zero even at $t_{cycle} = 1\,\mu s$ for minimal LT_{TX} as shown in Fig. 22. It is significantly lower than in always-on mode for low data rates.

VII. CONCLUSION

After studying general aspects of duty-cycling, relevant TX metrics and duty-cycling efficiency calculations are presented. The various aspects and necessary steps to assess the duty-cycling performance of PAs are reviewed and implementation for mmWave class-E PAs is studied. The internal turn-on behavior is separated into two aspects, OPS and large-signal swing-in, and partially accelerated using a kick-starter circuit. A two stage 14 dBm V-band

PA is designed in a 130 nm SiGe process and detailed measurements of the duty-cycling behavior are reported. For this, a dedicated broadband amplifier based on an off-the-shelf operational amplifier is used to obtain a rise time of 1 ns at the 50 Ω 1.5 V enable input. During turn-on, sub-nanosecond delay and rise times are achieved, but depending on the system requirements, the total turn-on time is dominated by the settling behavior in nanoseconds range. In measurements with 1 GBaud-GMSK, the proposed PA delivers the desired output signal quality after 2 ns. Thus, the power consumption almost linearly scales with data rate, even when aggressively duty-cycling the system with a $t_{\text{cycle}} = 1\,\mu\text{s}$ for minimum LT_{TX}. The measured P_{sleep} is more than 10^6 times smaller than P_{idle}. This top-down study allows system and circuit designers to better evaluate requirements and performance for switchable PAs in context of duty-cycled communications. It enables further studies on integration of such in practical transceiver systems focusing on necessary protocol changes, on duty-cycling of additional TX blocks and on further aspects of PA design such as temperature-compensated biasing.

APPENDIX
BUTTERWORTH FILTER RESPONSE

In the following, the response of the 2nd order Butterworth bandpass filter to a stepped sine input is derived: The bandpass has a center frequency f_c, the corresponding angular center frequency $\omega_c = 2\pi f_c$ and a quality factor Q, resulting in a bandwidth $B_{\text{BP}} = \frac{f_c}{Q}$. In the following, s is the Laplace transform parameter and t the time-domain parameter. Since we are only interested in distortion of the envelope of the RF-signal, we analyze this in baseband. Here, the stepped sine is only a step represented by $S(s) = \frac{1}{s}$ and the bandpass filter acts as a lowpass filter with bandwidth $B_{\text{LP}} = B_{\text{BP}}/2$. Based on the normalized transfer function $H_{\text{LP,n}}(x)$ for a 2nd order Butterworth lowpass filter described by [51]

$$H_{\text{LP,n}}(x) = \frac{1}{x^2 + \sqrt{2}x + 1}, \tag{8}$$

we derive the frequency domain representation $H_{\text{LP}}(s)$ by denormalizing it with $x = \frac{s}{2\pi B_{\text{LP}}} = 2Q\frac{s}{\omega_c}$:

$$H_{\text{LP}}(s) = \frac{1}{\frac{4Q^2s^2}{{\omega_c}^2} + \frac{2\sqrt{2}Qs}{\omega_c} + 1} \tag{9}$$

The filter output in time domain $a(t)$ is calculated by inverse Laplace transformation of the filter product:

$$a(t) = \mathcal{L}^{-1}\{H_{\text{LP}}(s) \cdot S(s)\} \tag{10}$$

$$= 1 - \cos\left(-\frac{1}{4}\pi + \frac{\sqrt{2}\omega_c t}{4Q}\right)\sqrt{2}e^{\left(-\frac{\sqrt{2}\omega_c t}{4Q}\right)} \tag{11}$$

In Fig. 23, the analytical baseband response based on (11) is compared with the numerically determined bandpass filter response at RF.

We want to determine the time $T_{\text{d,BP}}$ after which the envelope is distorted by less than 1 %. To simplify analytical evaluation, we only consider the exponential decay factor $b_{\text{exp}}(t)$:

$$b_{\text{exp}}(t) = \sqrt{2}e^{\left(-\frac{\sqrt{2}\omega_c t}{4Q}\right)} \tag{12}$$

If $b_{\text{exp}}(T_{\text{d,BP}}) = 1\,\%$, the combined distortion $(1 - a(t)) \leq 1\,\%$ for $t \geq T_{\text{d,BP}}$, because $|\cos| \leq 1$. Solving $b_{\text{exp}}(T_{\text{d,BP}}) = 1\,\%$ for $T_{\text{d,BP}}$ yields

$$T_{\text{d,BP}} = \frac{2\sqrt{2}Q\log\left(100\sqrt{2}\right)}{\omega_c} = \frac{\sqrt{2}\log\left(100\sqrt{2}\right)}{\pi B_{\text{BP}}}, \tag{13}$$

which is inversely proportional to B_{BP}.

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