Analysis and design of a 55–74 GHz ultra-compact low-noise amplifier using highly asymmetric transformers

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This letter presents a low-noise amplifier with a 3 dB-bandwidth, from 55 to 74 GHz, excellent noise performance and low power consumption based on a three-stage common-source topology. For the first time to the authors' best knowledge, an analytical equation that also considers the gate–drain capacitance is derived for the employed shunt–series transformer feedback input matching network. To enable shunt–series transformer feedback matching without significant gain reduction a highly asymmetric transformer is designed. Furthermore, a compact transformer-implemented T-shaped output matching network is investigated to minimize the required area. To prove these concepts, the circuit has been fabricated in a 22 nm fully depleted silicon-on-insulator technology. Thanks to the transformer-based matching, an ultra-compact active footprint of 0.039 mm^2 is achieved. At a power consumption of 8.4 mW from a 0.41 V supply an average noise figure of 4.8 dB and a peak gain of 14.2 dB has been measured. In- and output matching better than −10 dB over the 19 GHz wide 3 dB-bandwidth are demonstrated.

Introduction: Due to the large available bandwidth and the use of small passive components, the V-band (40 to 75 GHz) is well suited for high-data-rate applications in directional [1–3] or wireless body-area network (WBAN) systems [4, 5]. Both applications require compact and low-power front-ends, usually incorporating a low-noise amplifier (LNA) in the receiver. While transmission-line-based LNA designs are more commonly used in the V-band [6–8] due to faster design times, lumped matching can reduce the chip size significantly and transformers can additionally improve performance [9–14]. For these it is important to have accurate design equations to accelerate the design phase. Accordingly, [13–16] analytically evaluates the commonly used shunt–series transformer feedback (SSTF) input matching network for a common-source (CS)-stage. However, the gate–drain capacitance C_{gd}, which has a significant impact in V-band designs in advanced technologies, is always neglected in these analytical approaches.

Therefore, this letter analyses the SSTF network considering C_{gd} and presents the design of a required highly asymmetric transformer. Additionally, a compact transformer-implemented T-shape output matching network and the corresponding design equations are investigated. To prove the concept, the circuit is fabricated in a 22 nm fully depleted silicon-on-insulator (FD-SOI) technology, which is ideal for millimeter-wave (mmWave) CMOS LNAs [8, 17–19].

Circuit design: The proposed LNA is shown in Figure 1. It consists of three CS-stages, which were chosen over the commonly used cascode structure due to lower noise [20] and the smaller required supply voltage.

Transistor biasing and sizing: The transistor finger width and drain current density have been chosen for a minimum noise figure at a high f_{max}. The effective total width is dimensioned to achieve a 50 Ω real part of the optimum noise impedance. This width is split over multiple devices to minimize the gate resistance [19] without significantly increasing the parasitic capacitances. A positive back-gate voltage V_b reduces the threshold voltage allowing to use a single voltage of only 410 mV for the front-gate voltages V_{g1} and V_{g2}, V_b and the supply voltage V_{dd} while maintaining the desired drain current. Local AC-shunt capacitors are employed for V_{g1} and V_{g2}. The pad-connection of V_{g1}, V_{g2} and V_{dd} is implemented using 0 Ω-lines [6, 21].

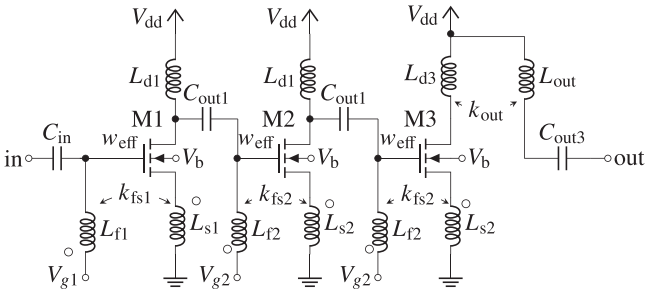


Fig. 1 *Schematic of the proposed LNA with shunt–series transformer feedback based on [14]*

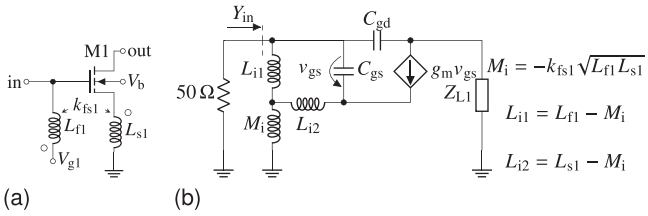
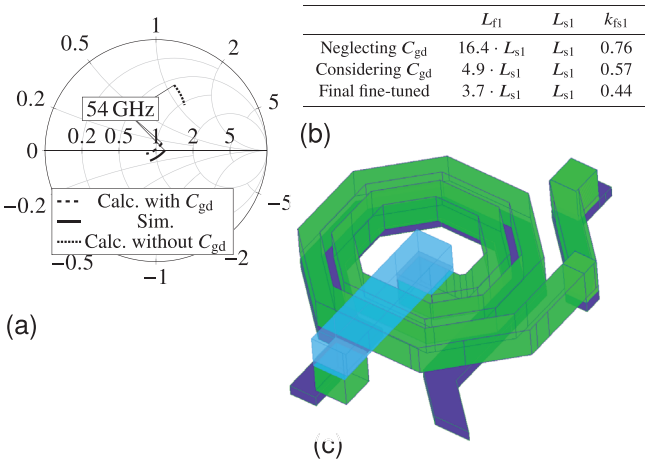


Fig. 2 *(a) Input CS-stage with shunt–series transformer feedback [14] and (b) its small-signal equivalent circuit with 50 Ω source and load Z_{L1}*

Shunt–series transformer feedback matching: To achieve a broadband simultaneous noise and power input match at a small footprint a SSTF network shown for the input stage in Figure 2a is used. From the simplified small-signal equivalent circuit considering C_{gd} with load Z_{L1} as shown in Figure 2b, an analytical formula for the input admittance has been derived and is shown in Equation 1, where $\sigma = 1 - k_{fs1}^2$. The required values of the transconductance g_m as well as C_{gd} and the gate–source capacitance C_{gs} of the equivalent circuit have been extracted from simulation of the properly biased and sized transistor using the PDK transistor compact model. To determine the transformer characteristics required for power matching to a 50 Ω source at 61 GHz, the reflection coefficient resulting from Equation 1 has been derived and numerically minimized within a range of L_{f1}, L_{s1} and k_{fs1} that is realizable on chip and limits the gain degradation due to source degeneration to a reasonable amount. With the determined optimum values the input impedance of the stage has been calculated and simulated. The results are compared in Figure 3a and show good agreement, whereas there is a significant deviation if neglecting C_{gd}. Figure 3b compares these determined optimum values with the, consequently very different, transformer characteristics calculated when neglecting C_{gd}; and with the final fine-tuned values after considering layout parasitics. Hence, Equation 1 enables quick but accurate results without requiring time consuming optimization based on circuit simulations.

Subsequently, an appropriate transformer shown in Figure 3c has been designed utilising EM-simulations. To achieve the desired high coupling coefficient of the two very different inductances, a stacked design is

$$Y_{in} = \frac{+j\left[-\left(L_{f1}L_{s1}g_m\sigma + 2\sqrt{L_{f1}L_{s1}}C_{gs}Z_{L1}\sqrt{1-\sigma} + (L_{f1}+L_{s1})C_{gs}Z_{L1}\right)C_{gd}\,\omega^3 + \left(C_{gd}Z_{L1} + L_{s1}g_m + \sqrt{L_{f1}L_{s1}}g_m\sqrt{1-\sigma}\right)\omega\right]}{\left[C_{gd}C_{gs}L_{f1}L_{s1}Z_{L1}\sigma\,\omega^4 - \left(L_{s1}g_m\sigma + C_{gd}Z_{L1}\right)L_{f1}\omega^2\right] + j\left[-\left(C_{gd}Z_{L1}g_m + C_{gs}\right)\sigma L_{f1}L_{s1}\,\omega^3 + L_{f1}\,\omega\right]} \quad (1)$$



	L_{f1}	L_{s1}	k_{fs1}
Neglecting C_{gd}	$16.4 \cdot L_{s1}$	L_{s1}	0.76
Considering C_{gd}	$4.9 \cdot L_{s1}$	L_{s1}	0.57
Final fine-tuned	$3.7 \cdot L_{s1}$	L_{s1}	0.44

Fig. 3 *(a) Comparison of input impedance of CS-input stage from 54 to 75 GHz calculated with Equation 1 and simulated with PDK transistor model; (b) Obtained transformer characteristics; (c) Final fine-tuned transformer layout*

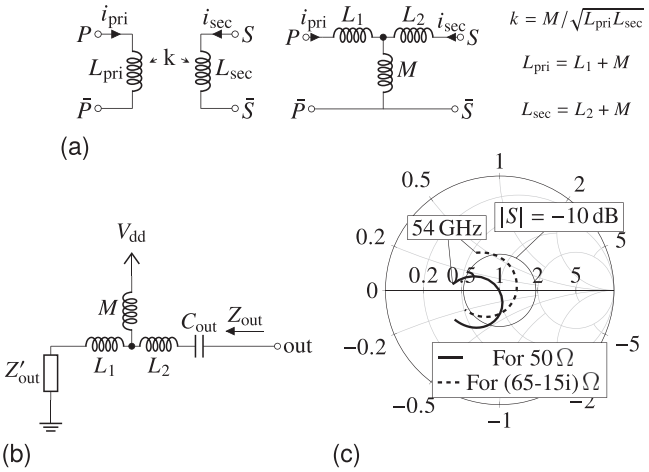


Fig. 4 *(a) Ideal transformer and its equivalent circuit; (b) T-shaped inductor network for broadband output match; (c) Simulated output impedance from 54 to 75 GHz of proposed LNA with different matching networks*

employed and the L_{f1} spiral is routed twice over a very wide L_{s1} coil. This leads to a lower quality factor compared to single inductors, but the resulting increase in NF is compensated by the inherently better noise performance of SSTF matching compared to simple inductive degeneration [15, 22]. The DC blocking capacitance C_{in} shifts the match centre from 61 to 52 GHz. The proposed LNA is well noise-matched over the 3 dB-bandwidth with less than 0.15 dB of NF attributed to noise mismatch according to simulation.

The output of the first two stages was initially matched to 50 Ω using a simple LC-network and for input matching of the consecutive stages the same SSTF network was employed. Starting from this, the inter-stage matching has been optimized using simulations to improve the bandwidth. Input and output impedance of a stage have a roughly conjugate complex frequency behaviour, resulting in a broadband matching.

Transformer-based T-network: For a broadband 50 Ω output match a T-shaped inductor network implemented as a single transformer is employed. Figure 4a shows an ideal transformer with primary inductance L_{pri}, secondary inductance L_{sec} and a coupling coefficient k and its equivalent circuit with the inductances L_1, L_2 and M. Based on the respective equations any T-shape inductor network can be emulated with a transformer. This reduces the required area to almost a third. When transforming the output impedance of the gain stage Z'_{out} with the proposed matching network shown in Figure 4b, the combined impedance Z_{out} reads

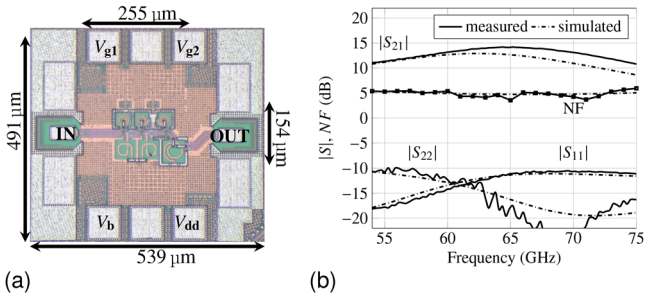


Fig. 5 *(a) LNA die photograph; (b) S-parameters and noise figure of proposed LNA*

$$Z_{out} = \frac{1}{j\omega C_{out}} + j\omega L_2 + \frac{1}{\frac{1}{Z'_{out}+j\omega L_1} + \frac{1}{j\omega M}}$$

$$= \frac{-\omega M\left(\mathrm{Im}(Z'_{out}) + \omega L_1\right) + j\omega M\,\mathrm{Re}(Z'_{out})}{\mathrm{Re}(Z'_{out}) + j(\omega(L_1+M) + \mathrm{Im}(Z'_{out}))}$$

$$+ j\left(\omega L_2 - \frac{1}{\omega C_{out}}\right). \quad (2)$$

It should be noted that this network only matches capacitive outputs since the real part of Equation 2 is only positive for $\mathrm{Im}(Z'_{out}) < 0$. When conjugate complex matching this to a load Z_L at the angular centre frequency ω_c there are two degrees of freedom. One degree is removed by choosing $L_1 + M = -\frac{\mathrm{Im}(Z'_{out})}{\omega}$ which simplifies the analytical evaluation. Applying this to Equation 2 and considering the real and imaginary valued parts separately, allows calculating M and subsequently C_{out} as

$$M = \frac{1}{\omega_c}\sqrt{\mathrm{Re}(Z_L)\,\mathrm{Re}(Z'_{out})}, \quad (3)$$

$$C_{out} = \frac{1}{\omega_c(\omega_c(M+L_2) + \mathrm{Im}(Z_L))}. \quad (4)$$

With the remaining degree of freedom L_2 could be set to zero. However, simulations show that a non-zero value for L_2 can result in a more broadband match because it partially compensates the change of Z_{out} due to C_{out} over frequency.

The proposed LNA is connected to a 50 Ω load, but the matching bandwidth can be further increased by targeting a more resistive and capacitive value for Z_L in Equations 3, 4 at the cost of a worse match at the centre frequency. This is visualized in Figure 4c which shows the output impedance of the LNA with $L_2 = 40$ pH matched with the proposed network designed for $Z_L = 50$ Ω as well as for $Z_L = (65 - 15i)$ Ω at ω_c. Ultimately, a much broader matching compared to a basic LC-network is achieved at a similar footprint.

Measurements: To prove the aforementioned concepts, a chip was fabricated and experimentally characterized on-wafer in a laboratory. The fabricated chip is shown in Figure 5a and measures 539 μm × 491 μm including pads while the core area is only 255 μm × 154 μm. V_{dd}, V_{g1}, V_{g2} and V_b have separate DC pads only for testing purpose. The LNA draws 20.5 mA from the 0.41 V supply. The S-parameter was measured with a 110 GHz vector network analyser. The NF measurements have been conducted separately above and below 60 GHz through the standard Y-factor method using a suitable noise source. Above 60 GHz, a custom E-band receiver has been used for detection.

Figure 5b shows the measured and simulated S-parameters and noise figure. The LNA exhibits a peak gain of 14.2 dB at 65 GHz. The 3 dB-bandwidth is 19 GHz from 55 to 74 GHz with both $|S_{11}|$ and $|S_{22}|$ below −10 dB. The minimum NF is 3.5 dB while the average NF within the 3 dB-bandwidth is 4.8 dB. The input 1 dB-compression point at 65 GHz is −17.5dBm. Table 1 compares the results against state-of-the-art V-band CMOS LNAs.

Conclusion: Targeting a wideband low-noise design, the commonly used SSTF input matching network has been analysed also considering, for the first time to the authors' best knowledge, C_{gd}. To enable this

Table 1. Comparison with state-of-the-art V-band CMOS LNAs

	Tech	f_c[1]/GHz	V_{dd}/V	Gain/dB	min./avg.[2]NF/dB	BW[3]/GHz	P_{dc}/mW	IP_{1dB}/dBm	Area (core)/mm^2	FoM[4]
[14] MWCL 2012	90 nm CMOS	5	1	12.5	5.4/5.9[5]	6	4.4	−16	0.36 (0.047)	50
[12] ELL 2015	65 nm CMOS	62	1	30	4.6/4.7[5]	3.5[5,6]	8.9	−30	0.49 (0.12[5])	6
[23] ELL 2017	65 nm CMOS	56	1	14.9	5.7/6.1	16.7[7]	9.6	−21.4	0.59 (0.084[5])	23
[10] JNM 2019	65 nm CMOS	57	1	17.4	4/4.3[5]	10.9	10	−14.5	0.26 (0.095[5])	169
[24] BCICTS 2019	45 nm RF-SOI	64	1.2	22.2	3.3[5]/NA	31[8]	30	−21.8	NA (1.13)	NA
[8] MWCL 2021	22 nm FD-SOI	59	0.85	18.1	4.4/4.9	18.3[9]	3.6	−21.1	0.39 (0.24[5])	152
[11] MWCL 2022	28 nm CMOS	73	1.4	13.48	4.56/5.4[5]	6.6	3.64	−19.2	0.28 (0.088)	42
This work	22 nm FD-SOI	64	0.41	14.2	3.5/4.8	19	8.4	−17.5	0.26 (0.039)	102

[1]centre frequency [2]average over BW [3]3 dB-bandwidth [4]FoM $= \frac{\text{Gain[lin.]}\cdot IP_{1dB}\text{[mW]}\cdot\text{BW[MHz]}}{P_{dc}\text{[mW]}\cdot(F\text{[lin.; avg.]}-1)}$ [5]estimated from figure [6]$|S_{11}| \not< -10$ dB [7]$|S_{11}| < -10$ dB only over 12 GHz of BW [8]$|S_{11}| < -10$ dB only over 17 GHz of BW [9]$|S_{11}| < -10$ dB only over 7 GHz of BW.

SSTF matching of CS-stages without considerable gain degradation, a compact very asymmetric transformer has been designed. Additionally, a compact transformer-based output matching network has been investigated. To prove the concept, an ultra compact low-power LNA has been demonstrated in a 22 nm FD-SOI technology. The proposed LNA covers the unlicensed bands between 55 and 74 GHz with a peak gain of 14.2 dB, an NF between 3.5 and 5.7 dB and input and output matching better than −10 dB.

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Conflict of interest: The authors declare no conflict of interest.

Data availability statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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